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EVALUATION OF FLUORENE POLYESTER FILM CAPACITORS (PREPRINT)

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14. ABSTRACT
Next generation electrical power systems are being packaged into more compact, power dense architectures as means to improve the performance of electrically-driven technologies. This trend has increased the demand for efficient high voltage power devices that are operable under austere conditions. The capacitive component is commonly identified as a limiting technology with respect to operational use temperature and/or self-heating. Recent industrial processing and metallization of fluorene polyester (FPE) films (Tg ~ 330°C) has enabled the manufacturing of wound capacitors that are more temperature tolerant. While a high Tg polymer film capacitor is expected to have thermally stable electronic properties, the performance will also be dependent on the architecture and packaging. A modeling and simulation capability is utilized herein to investigate the device architecture-electrical performance relationships for packaged and unpackaged FPE film capacitors. Initially, a mathematical model was developed for both equivalent capacitor circuit analysis and device architecture field analysis, which were used to identify factors that affect device properties. Additionally, finite element analysis of selected device architectures was accomplished to compare magnetic fields and thermal profiles predicted. The electrical properties of packaged and unpackaged FPE devices were then evaluated under stressed conditions, to include cycling from ambient to 200 °C.

15. SUBJECT TERMS
Fluorene polyester, Capacitor, Packaging, High Temperature, DC/DC converter

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Evaluation of Fluorene Polyester Film Capacitors

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Next generation electrical power systems are being packaged into more compact, power dense architectures as means to improve the performance of electrically-driven technologies. This trend has increased the demand for efficient high voltage power devices that are operable under austere conditions. The capacitive component is commonly identified as a limiting technology with respect to operational use temperature and/or self-heating. Recent industrial processing and metallization of fluorene polyester (FPE) films (T_g ~ 330°C) has enabled the manufacturing of wound capacitors that are more temperature tolerant. While a high T_g polymer film capacitor is expected to have thermally stable electronic properties, the performance will also be dependent on the architecture and packaging. A modeling and simulation capability is utilized herein to investigate the device architecture-electrical performance relationships for packaged and unpackaged FPE film capacitors. Initially, a mathematical model was developed for both equivalent capacitor circuit analysis and device architecture field analysis, which were used to identify factors that affect device properties. Additionally, finite element analysis of selected device architectures was accomplished to compare magnetic fields and thermal profiles predicted. The electrical properties of packaged and unpackaged FPE devices were then evaluated under stressed conditions, to include cycling from ambient to 200 °C.

Key words: Fluorene polyester, Capacitor, Packaging, High Temperature, DC/DC converter

I. Introduction

For many applications, electrical systems continue to evolve into higher power, more compact architectures as a means to increase performance and enhance capability. In particular, there has been a concerted effort in the aviation community to develop "more electric" architectures as a means to improve the capability, reliability, and maintainability of the aircraft [1], [2]. Continued progression of these developments is constrained by the ability to thermally condition the electrical subsystems in a harsh environment. An approach to ease this constraint is to develop thermally robust electrical systems to reduce the thermal load to the heat pump and to enable placement of electrical technology in close proximity to heat sources (e.g., generators, motors, leading).

Capacitors are commonly identified as a limiting component within the electrical power conditioning system due to the low volumetric energy density, narrow operational temperature range, and high production cost [3]. The desire to raise the upper temperature limit for capacitors has grown significantly due to recent progress in silicon carbide

technology [4], high-temperature magnetic material development [5], and the demonstration of these components into power electronics for operation at temperatures above 200°C [6]. While a variety of ceramic-type devices [7,8] and stacked inorganic thin film capacitors [9,10] have demonstrated promising results, high-temperature polymer film capacitors tend to have desirable features such as graceful failure and roll-to-roll production capability. Of interest is the recent manufacturing of fluorene polyester film at the industrial scale for capacitor fabrication due to its high glass transition temperature and low dielectric loss tangent [11]. Metalized FPE film was therein wound at a high yield to fabricate 7-11 µF capacitors with a breakdown strength >200 V/µm, a low dissipation factor (~1 %), and a high insulation resistance (>25,000 MΩ)[12]. These capacitors withstood lifetime tests of 250 hours at 200 ^{o}C and 250 V_{DC}, demonstrating their ability to withstand high voltage and temperature conditions.

The availability of FPE film is expected to improve the capability to fabricate polymer film capacitors that can withstand exposure to high temperature environments and/or tolerate internal heating due to power dissipation, but other encompassing capacitor performance requirements (e.g., *ESR*, *ESL*, efficiency, internal heating) may need to be addressed for proper integration into developing power systems. This integration would require an in-depth analysis of the capacitor architecture to include material components and their respective thickness since it is expected to have a notable impact on the device performance and therefore limit its potential application [13,14]. This knowledge could be applied to identify whether requirements such as voltage withstand strength, temperature cycling, energy storage, and graceful failure can be obtained while still maintaining a low equivalent series resistance and inductance.

Both packaged and unpackaged FPE capacitors are evaluated herein via modeling, simulating, and testing techniques so as to gain a better understanding of their applicability for use in high power electrical systems at high temperature. In particular, the devices are evaluated for use as an output filter capacitor in a high switch rate interleaved boost converter. A simplified equivalent circuit is initially utilized to define the properties of the capacitors, which are then incorporated into simulations generated with finite element method software. The simulations are then used to evaluate the magnetic fields and thermal profile for both capacitor architectures as a means to study the parasitic inductance and heat dissipation. Next, a combination of the modeling and simulation results are then correlated with empirical data obtained from the testing of prototype capacitors up to 200 °C. Finally, these learned characteristics are utilized with a converter simulation to evaluate the performance of the fluorene polyester (FPE) capacitors under high power, high frequency AC excitations.

II. Capacitor Modeling for ESR and DF

By solving the capacitor equivalent circuit model shown in Figure 1, a simplified representation of the equivalent series resistance (*ESR*) and dissipation factor (*DF*) can be derived.

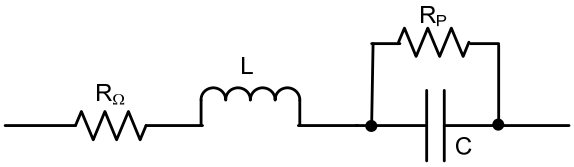


Figure 1. Equivalent circuit model of a capacitor.

In the above model[15], R_P represents the dielectric and absorption loss. For this study, the R_p is treated as a true resistance, and the change in capacitance with frequency is neglected. These assumptions may need to be addressed with further modification of the above model. R_Ω represents the ohmic loss. The ohmic losses are contributed by electrode resistance as well as various manufacturing-specific resistances such as electrodes, solder termination resistance, lead resistance, and resistive loss due to fringing field from the dielectric. From this circuit model, the total circuit impedance (Z_{cap}) is expressed in Equation 1.

$$Z_{cap} = \left(R + \frac{R_P}{1+\omega^2 C^2 {R_p}^2}\right) + j\left(\omega L - \frac{\omega C R_P^2}{1+\omega^2 C^2 {R_p}^2}\right) \quad (1)$$

Using Equation 1, the expression for *ESR* is defined.

$$ESR = R_{\Omega} + \frac{R_P}{1+\omega^2 C^2 {R_p}^2} \tag{2}$$

If the capacitor is good and not leaky, $\frac{1}{\omega C} \ll R_p$, then

$$ESR = R_{\Omega} + \frac{1}{\omega^2 C^2 R_p}\left(1 - \frac{1}{\omega^2 C^2 {R_p}^2}\right) \tag{3}$$

and also reactance *X*, which is the imaginary part of Z_{cap} becomes

$$X = \omega L - \frac{1}{\omega C}\left(1 - \frac{1}{\omega^2 C^2 {R_p}^2}\right) \tag{4}$$

Several equivalent circuit models have been proposed to properly fit impedance spectroscopy data for dielectrics and capacitors and have been shown to influence the outcome of the analysis [16]. The desire is to develop an ideal model to represent the real value (*ESR*) and imaginary value (reactance) obtained from the impedance measurements wherein it is possible to derive all four values in the capacitor equivalent circuit (Figure 1). Typically, a simplified equivalent circuit model (e.g., capacitor in series or parallel to a resistive component) can provide a good representation of the device properties when used under controlled conditions. However, as the environmental temperature, electric field strength, signal intensity, or frequency limits are modified, the use of these simplified models can result in gross misrepresentation of the device properties and expected performance. Examples include the appearance of fluctuations in capacitance at frequency due to inductance or variations in *ESR* due to a change in *C* or R_p. Currently, efforts to obtain all four component values inside a capacitor are underway and will be addressed in future studies.

III. Capacitor Architecture Study

In this paper, electrical and thermal performances of both unpackaged and packaged FPE cylindrical capacitor architectures were considered and evaluated. A pictorial view of the packaged and unpackaged capacitors is shown in Figure 2A. The surface outline diagram for the capacitor architectures considered is shown in Figure 2B. Initial finite element analysis (FEA) simulation, using the software QuickField Professional, was accomplished to predict temperature distributions and parasitic inductance. Since this software is 2-D FEA, both temperature and magnetic profiles were solved for the radial cross sections. The results of these simulations are shown in Table 1. It was assumed that 1 W of power was dissipated in the capacitors and the temperatures of the outer surface for both configurations were fixed at 300 K. For these results, only thermal conductions through the capacitors were considered as a means of heat removal. The equivalent thermal conductivity of the FPE dielectric film was assumed to be 0.2 W/mK. In addition, for the packaged capacitor the thermal conductivity of epoxy, which is used to fill the gap between outer package and the wound FPE film, is assumed to be 0.548 W/mK. The data in Table 1 predicts that the peak temperature rise is 8.8 K for the unpackaged capacitor, whereas the packaged capacitor shows a maximum temperature rise of 10.8 K. In terms of the equivalent series inductance (ESL), the unpackaged capacitor also provides a lower predicted ESL of 2.68 nH, whereas a predicted ESL of the packaged cylindrical geometries resulted in excess of 22.1 nH.

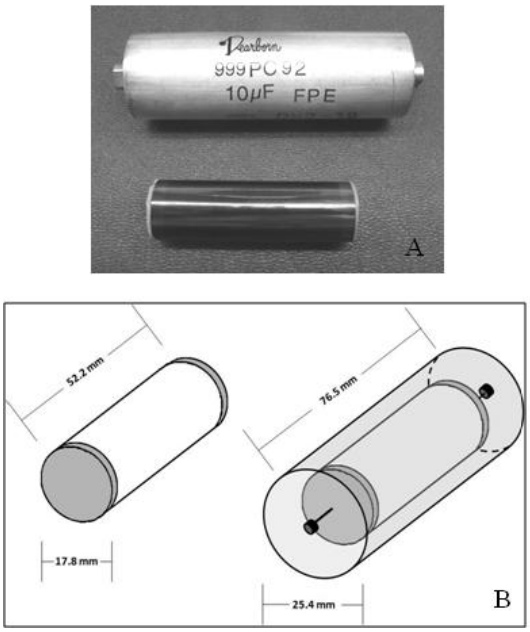


Figure 2. Images (A) and schematics (B) of 10 μF metallized FPE packaged (top) and unpackaged (bottom) capacitors studied for electrical and thermal performance evaluation.

Table 1. Summary of the finite element analysis results for the capacitor thermal and electrical performance

Capacitor Type	Unpackaged capacitor	Packaged capacitor
Package diameter (mm)	NA	25.4
Package length (mm)	NA	76.5
FPE wound capacitor diameter (mm)	17.8	17.8
FPE wound capacitor length (mm)	52.2	52.2
Dissipated power (W)	1	1
Thermal conductivity (W/mK)	0.2	0.2
Surface temperature (K)	300	300
Maximum temperature (K)	308.8	310.8
Inductance (nH)	2.68	22.1

A comparison of the simulated temperature distributions for the unpackaged and packaged capacitors is shown in Figure 3. As expected, it is shown that the packaged capacitor architecture has a higher internal temperature rise than the unpackaged one. This higher maximum internal temperature rise for the packaged capacitor is simply due to the additional thermal resistance of the epoxy. Conversely, since the unpackaged capacitor carries no external thermal resistance due to the epoxy part, the internal heat can be extracted more efficiently. The magnetic fields at the middle point along the capacitor length resulting from a simulated current of 1 A is shown in Figure 4. These devices have an outer layer, which represents a copper shroud that is wrapped around each device. The copper shroud is electrically connected to the device such that the current that goes into the device follows a path out through the shroud. This results in the magnetic field being essentially confined inside the capacitor. It should be noted that the magnetic fields of the wound FPE film sections are identical between the unpackaged and packaged capacitors. Therefore, the difference in inductance for both configurations is due to the extra sections of the packaged configuration. Since the magnetic fields and the inductance of the capacitor are related by Equation 5, the

lead sections and the epoxy section are responsible for the difference in inductance of the packaged capacitor compared to the unpackaged configuration.

$$\frac{1}{2}LI^2 = \frac{1}{2}\int \frac{B^2}{\mu} dv \tag{5}$$

(a) Unpackaged FPE capacitor

(b) Packaged FPE capacitor

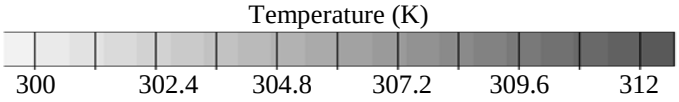
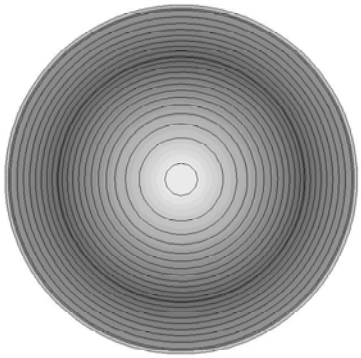


Figure 3. Temperature rise distribution for the four capacitor architectures dissipating 1 W of power.

I. Unpackaged FPE capacitor



II. Packaged FPE capacitor

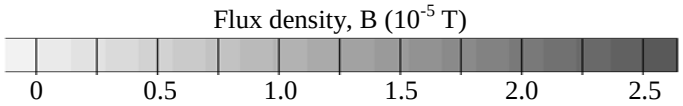


Figure 4. Magnetic field distribution for the packaged and unpackaged FPE capacitors with 1 A of current.

IV. Thermal and Electrical Performance of FPE Capacitors

Cylindrical, 10 μF metalized FPE film capacitors purchased from Dearborn Electronics, Inc. were experimentally characterized in terms of electrical and thermal performance. FPE dielectric film has highly desirable properties including a stable dielectric constant over wide frequency (up to 1 MHz) and temperature (up to 250 ^{o}C) ranges [12]. The images in Figure 2A are of a packaged as well as an unpackaged FPE capacitor used in this study. The diameter and length of the capacitors under study were 17.8 mm x 52.2 mm, respectively for the unpackaged wound capacitor and 25.4 mm x 76.5 mm for the packaged capacitor as depicted in the schematic diagram in Figure 2B.

The thermal experimental test was performed by wrapping the capacitor under test with silicon heat tape and placing the capacitor inside a thermally insulated box. Prior to wrapping the capacitor with heat tape, a thermocouple wire was mounted to the exterior diameter of the capacitor at the midpoint lengthwise and held in place with Kapton tape. The temperature was computer monitored and controlled to within ±1 °C of the set-point. At each temperature setting, the capacitor was heat soaked for 1 hour prior to performing the electrical measurements. The measurements were performed, without a copper tape shroud on the capacitor, using an Agilent 4284A LCR meter.

Figure 5 shows a plot of *ESR* at various temperatures as a function of frequency for the packaged capacitor. The *ESR* is initially high at low frequencies due to the influence of R_p and then decreases rapidly at higher frequencies to a stabilized value above 10 kHz. But upon evaluation at a lower scale in the insert of Figure 5, the *ESR* actually appears to increase again upon approaching 1 MHz. This initial increase in ESR shifts to a lower frequency, and the overall *ESR* value then increases steadily for each increase in temperature. For low frequencies, the *ESR* decreased as the temperature was increased from room temperature (20 °C) up to 100 °C and only a slight change occurs up to

150 °C. However, there is a notable increase in the *ESR* as the temperature increases from 150 °C to 200 °C. Similar observations were also observed with the ESR as the temperature was cycled back down. Additional temperature cycles then appeared to demonstrate an overall increase in the *ESR* as a function of frequency.

Figure 6 shows a similar *ESR vs. frequency* plot for the unpackaged capacitor. Similar trends are also observed for the *ESR* with temperature cycling. However, the value of *ESR* plateaued at a higher level (180 mΩ) and was attributed to the lower electrode thickness used for this device. The electrode resistivity for the unpackaged device was 40 Ω/sq vs. 15 Ω/sq for the packaged capacitor.

Based on the model in Figure 1 and Equation 2 above, the *ESR* of the capacitor is influenced either by R_Ω or by R_p, at an assumed fixed frequency and capacitance value. R_Ω represents connection and lead resistances while R_p represents internal resistances associated with the dielectric material, interfaces, or other factors due to the structure of the capacitor. If we assume a change in R_Ω is negligible, it is seen that the change is roughly proportional to $1/R_p$. Assuming *C* is constant with the temperature rise, increasing in *ESR* is due the reduction of R_p. In fact, preliminary investigation shows that the capacitance for FPE at 200 °C is almost unchanged from room temperature.

In Figure 5, it is apparent that as the temperature increases from room temperature up to 150 °C at low frequencies, the *ESR* decreased. Equation 2 would imply that this change in *ESR* is due to either to an increase in *C* or R_p as the temperature increased. However, as the temperature increased from 150 °C to 200 °C, the *ESR* value increased significantly, implying there was a corresponding decrease in the dielectric resistance of the capacitor. This response from 150 °C to 200 °C would follow standard reasoning that the dielectric film resistance decreases with an increase in temperature. This initial decrease in *ESR* followed by an increase was not observed at the higher frequencies, where the *ESR* increased steadily from room temperature up to 200 °C. The increase in *ESR* with temperature at high frequencies may be due to reactions with the electrode or a change in capacitance. Similar reasoning can be applied to the trends in *ESR* with temperature cycling in Figure 6 for the unpackaged device.

Evaluation of the *ESR* response at low frequencies indicates additional phenomena are possible. Simple suggestions could be desorption (outgassing) of water (or other organic vapors) as the temperature increases for the lower temperature changes, annealing of the dielectric, or as suggested by (Raju), α-relaxation, interfacial polarization, or ionic conductivity[16]. While these factors need to be explored further, the application of the model used would indicate that the insulation resistance of the dielectric may have a notable impact on the *ESR* at higher temperatures and fields for low frequencies.

Figure 7 shows the reactance as a function of frequency for the packaged capacitor. In this figure, the capacitor temperature was cycled from 20-200 °C. Arrow A in this figure shows the first cycling and Arrows B and C are the second and third cycling. The general trend of reactance for the packaged capacitor was increasing as more temperature cycles were performed. It indicates that the resonant frequency of the capacitor was reduced with additional cycles.

The imaginary term in Equation 1 above is the reactance term. Taking this portion of the equation and solving for the resonant frequency (equating this reactance term to 0) yields

$$\omega_{res} = \sqrt{\frac{1}{(L_s * C)} - \frac{1}{C^2 * R_p{}^2}} \tag{6}$$

The reduction of the resonant frequency at the elevated temperatures for the packaged capacitor described above can be explained by a reduction of R_p at elevated temperatures. As discussed earlier, the increase in *ESR* is due to the reduction of R_p. Similarly the reduction of R_p can reduce the resonant frequency of the capacitor as expressed in Equation (6) above. It should be noted that once R_p becomes comparable or lower than $1/\omega C$, then the capacitor is no longer usable.

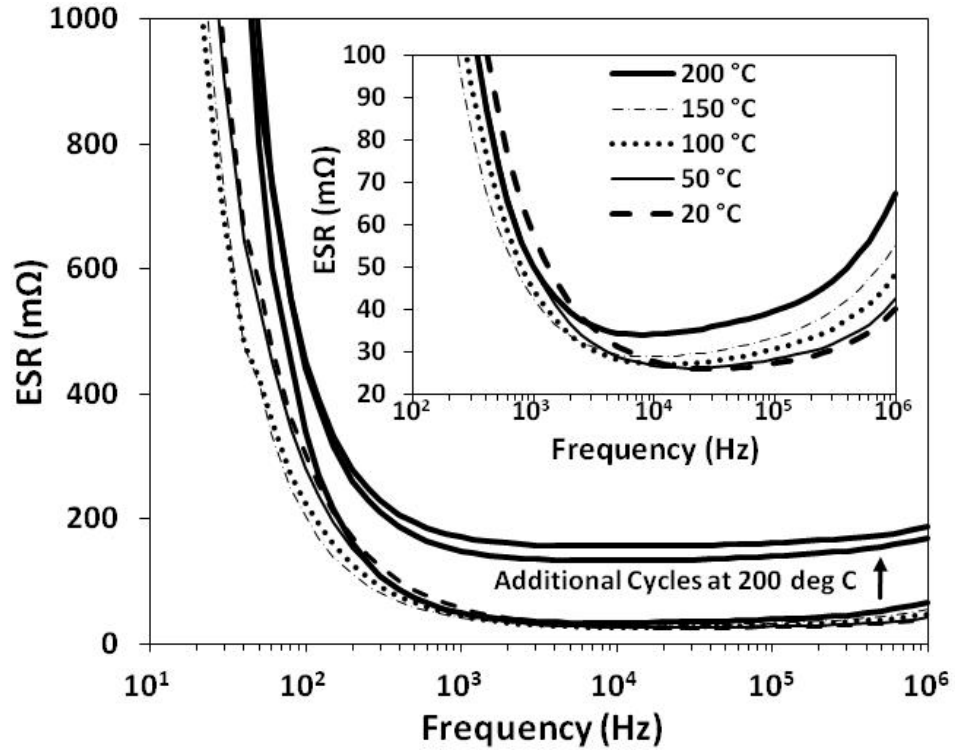


Figure 5. ESR vs. Frequency for Pkg'd Capacitor
(2nd cycle, 1 hr soak time, increasing temperature + other 200°C data from following cycles)

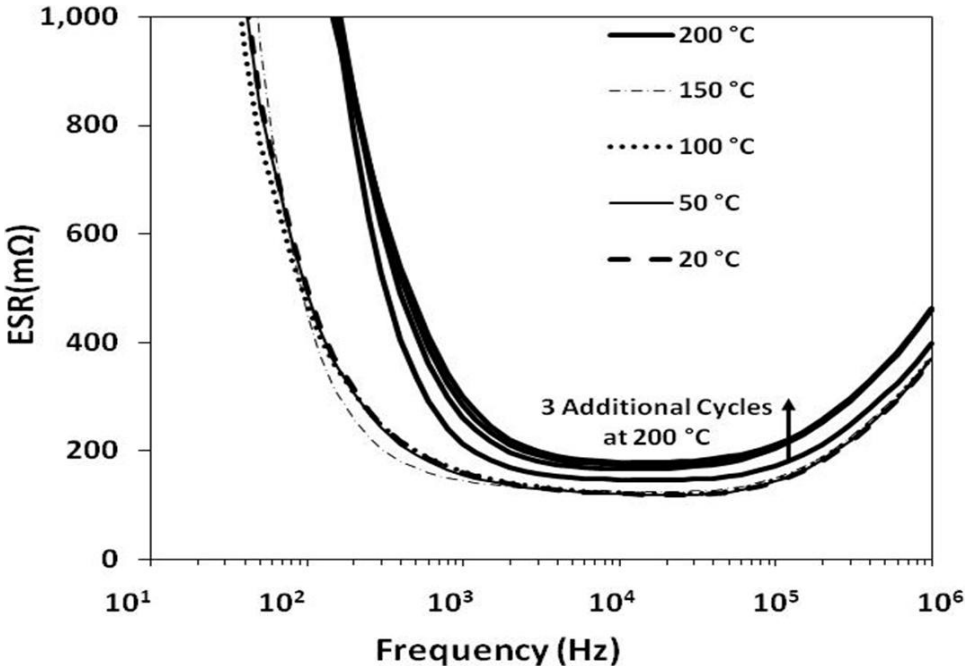


Figure 6. ESR vs. Frequency for UnPkg'd Capacitor
(Second cycle, 1 hr soak time, increasing temperature + other 200 °C data with following cycles)

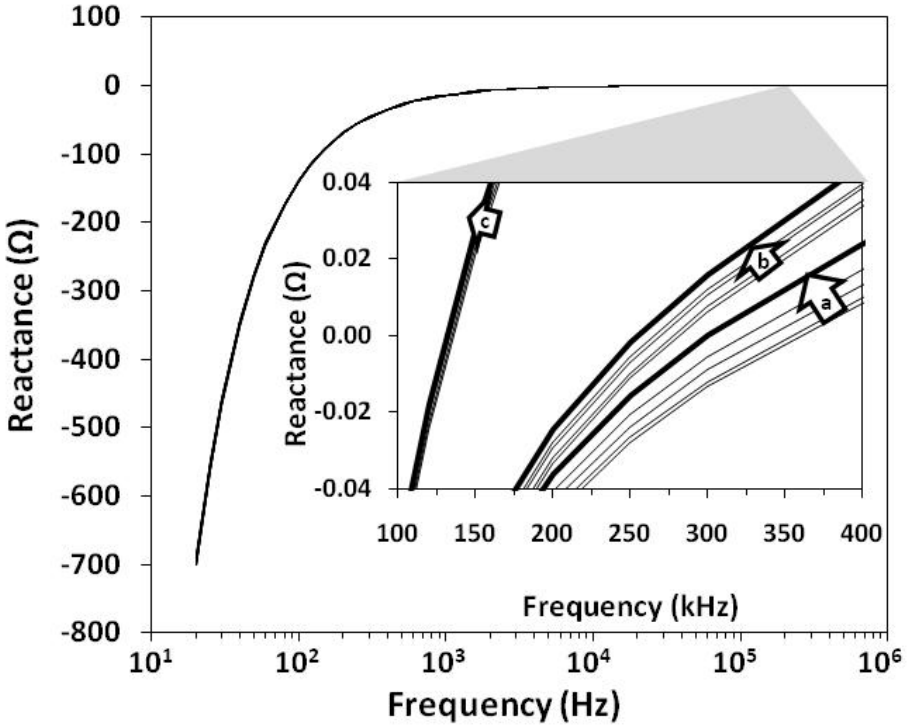


Figure 7. Reactance vs Frequency for Pkg'd Capacitor
(1 hour soak time at 20-200°C, multiple cycles)

V. Effect of ESR and ESL on Capacitor Power Loss and Temperature Rise, and Output Voltage Ripple in a DC/DC Converter Application

The *ESR* and *L* effect of a filtering capacitor on the output ripple voltage of dc/dc converters is considered next. Power dissipation in capacitors due to the ac current through it and the associated temperature rise are also discussed. Figure 8 shows an inverse-coupled two-phase interleaved dc/dc boost converter suitable for high performance and high power applications [17]. A 100 V/270 V, 10 kW boost converter with a duty ratio of 0.67 and a switch frequency of approximately 75 kHz is considered for evaluating the effects of an output filter capacitor's (C_{out}) *ESR* and *ESL* on the converter output ripple voltage and capacitor power loss and temperature rise.

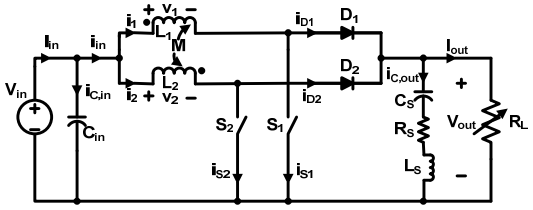


Figure 8. Circuit schematic of an inverse-coupled two-phase interleaved dc/dc converter.

For evaluating capacitor performance, four 10 μF FPE capacitors discussed in the previous section are considered. In this simulation, the capacitor was assumed to have R_s, L_s, and C_s as shown in Figure 8. R_s and L_s in this section are identical to R_Q and L used in Section II, but C_s is related to C mentioned in Section II by the expression (8)

$$C_s = \frac{1+\omega^2 C^2 R_p^{\ 2}}{\omega^2 C R_p^{\ 2}} \tag{7}$$

Since the interleaved converter described above works as a dual phase converter, the actual capacitor frequency is twice the operating frequency (150 kHz). Using SPICE simulation, the required total output filter capacitance to maintain ripple voltages to be 2.7V as a function of frequency is shown in Figure 9. As shown in the figure, the ripple voltages do not vary significantly with or without *ESR*. This means that the voltage across the *ESR* is very small since *I*ESR* is very small. Although it is not shown in the Figure, including inductance (22.1 nH for 10 μF) did not change the required capacitance values.

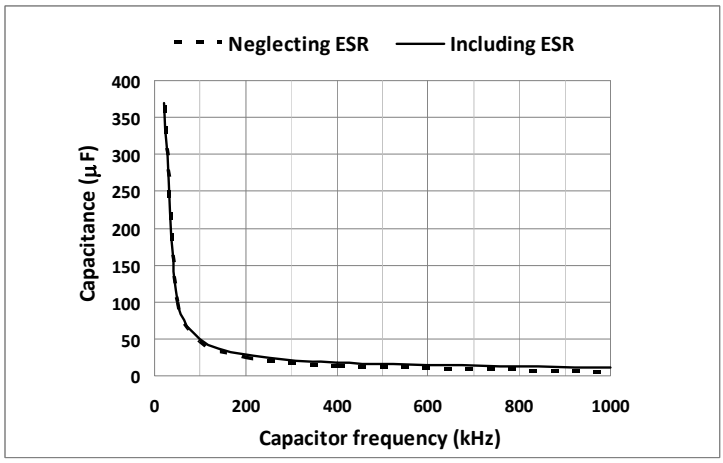


Figure 9. Required total output capacitance as a function of frequency when V_{pp} = 2.7 V. For this Figure, each 10 μF capacitor's ESR is assumed to be 30 mΩ.

Figure 10 shows the power dissipated in each capacitor as a function of *ESR* when a group of capacitors in parallel are used as the output capacitor for the DC-DC converter. Using the temperature rise as a function of power simulation results in Table 1 and the experimentally obtained *ESR* values, the internal temperature rise of the capacitor can be predicted. For a FPE packaged capacitor with *ESR* of 41.5 mΩ the dissipated power and the maximum internal temperature rise are 2.34 W and 24.3 K, if 4 capacitors are used in parallel. Further, the dissipated power and temperature rise for each capacitor for a group of six, eight and ten capacitors are 1.04 W (10.8 K), 0.59 W (6.1 K)and 0.37 W (3.8 K), respectively. For the unpackaged capacitor with 158 mΩ *ESR*, the corresponding values for each capacitor for 4, 6, 8 and 10 capacitors in parallel are 8.91 W (78.4 K), 3.96 W (34.8 K), 2.23 W (19.6 K), and 1.43 W (12.6 K), respectively. It should be mentioned that the power dissipation in each capacitor is proportional to the square value of the current, so that, for example, by multiplying the number of capacitors by a factor of two, the dissipation power on each capacitor will be reduced by a factor of four. These temperature rise values are very important especially, when these capacitors are designed for use in high temperature, high power systems.

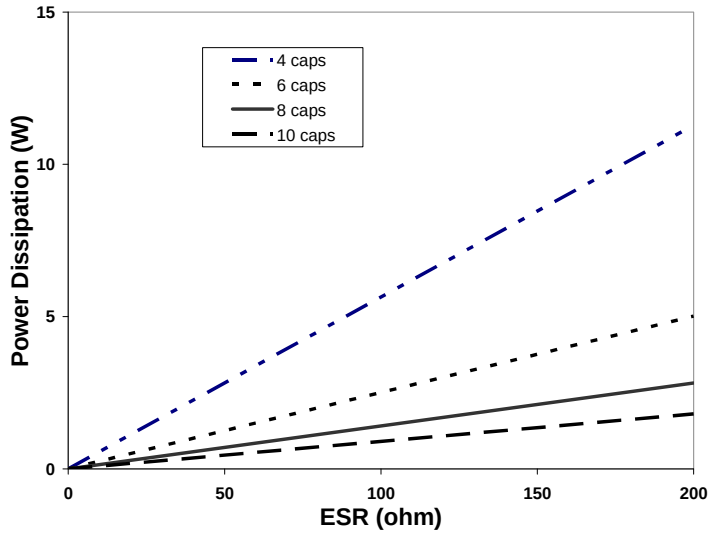


Figure 10. Power dissipation in an individual capacitor as a function of its ESR for various numbers of capacitor in parallel.

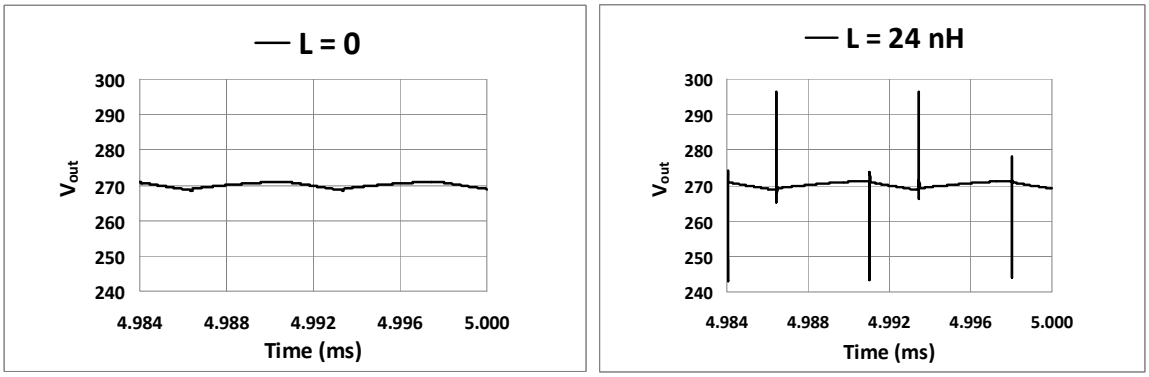


Figure 11. Effects of ESL on output voltage ripple of a 100 V/270 V, 10 kW, 75 kHz interleaved dc/dc converter. 4 -10 uF capacitors were connected in parallel. ESR of each capacitor was assumed to be 30 mΩ. (Left Figure: ESL=0 nH, Right Figure: ESL=24 nH)

Figure 11 shows the output noise is generated by the *ESL* in the capacitor. Although the bulk ripple voltage is almost identical with and without *ESL* in the capacitor, the harsh noises are present for the case with *ESL*. This condition takes place when the direction of current into the capacitor changes. At that time, *L*di/dt* becomes very large. From Figure 11, reducing the internal inductance of the capacitor is very important for not only increasing the operating frequency of the capacitor but reducing the unnecessary noise.

VI. Conclusions

Using modeling and simulation, an accurate estimate of a capacitor's equivalent series inductance and temperature rise were achieved and experimentally verified using an FPE capacitor. Both packaged and unpackaged FPE capacitor configurations were studied with simulation results indicating that the reducing *ESR* and *ESL* is necessary in terms of minimizing output noise and temperature rise. A methodology to evaluate the electrical and thermal performance of a capacitor in a dc/dc converter application using both finite element analysis and SPICE simulation packages is established. The importance of a low *ESR* and *ESL* capacitor design is highlighted for a high

temperature, high power and high performance dc/dc power converter application. Using the tools presented in this paper, it is possible to predict how a capacitor will perform thermally and electrically within a power converter system.

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